REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have incorporated the subject matter of claims 105 and 106 into claim 103; and, correspondingly, have cancelled claims 105 and 106 without prejudice or disclaimer. In addition, Applicants have further amended claim 103 to recite that "cobalt" silicide layers are formed in the surface of the semiconductor regions and the conductive film; and, in light thereof, have cancelled claims 109 and 120 without prejudice or disclaimer, and have amended the dependency of claim 110. Moreover, Applicants have further amended claim 103 to recite that the removal of the top of the semiconductor substrate and of the top of the conductive film is by "Ar" sputter-etching; and, light thereof, have cancelled claim 119 without prejudice or disclaimer. Furthermore, Applicants have amended claim 114 to recite the semiconductor "substrate", consistent with the parent claim thereof; and have amended claim 116 to be dependent on claim 115, rather than on claim 114.

Applicants have amended independent claim 124 to recite that the removal of the top of the second source/drain regions and of the top of the gate electrode is by "Ar" sputter-etching; to recite that a "cobalt" layer is deposited, with "cobalt" silicide layers being formed; and to recite that the cobalt silicide layers are not in contact with junctions formed by the first source/drain regions and the semiconductor substrate, whereby a current leakage between the cobalt silicide layers and the junctions is prevented. In light of amendments to claim 124, claims 125 and 126 have been cancelled without prejudice or disclaimer.

Moreover, claim 127 has been amended to recite that the removing the top of the second source/drain regions and removing the top of the gate electrode are by

"Ar" sputter-etching, and to recite that "cobalt" silicide layers are formed in the surface of the second source/drain regions and the gate electrode. In light of amendments to claim 127, claims 128 and 129 have been cancelled without prejudice or disclaimer, and dependency of claim 130 has been amended.

Furthermore, claims 139-144 have been cancelled without prejudice or disclaimer.

In addition, Applicants are adding new claims 145-148 to the application. Claims 145 and 146, each dependent on claim 103, respectively recites that the second semiconductor regions are formed to a depth of approximately 150 nm from the top of the semiconductor substrate, and recites that the second semiconductor regions are formed to a depth of 50-150 nm from the top of the semiconductor substrate. Note, for example, pages 17 and 24 of Applicants' substitute specification, submitted with the Preliminary Amendment filed November 27, 2001, in the above-identified application (hereinafter "Applicants' substitute specification"). Claims 147 and 148, dependent respectively on claims 103 and 147, respectively recites that in forming the cobalt silicide layers in the surface of the semiconductor regions, the bottom thereof is formed to be even; and recites that in forming the cobalt silicide layers in the surface of the semiconductor regions, a thickness thereof is uniform. Note, for example, paragraphs [0059]-[0061] on pages 23 and 24 of Applicants' substitute specification.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the documents applied by the Examiner in rejecting claims in the Office Action mailed May 20, 2005, that is, the teachings of the U.S. Patents to Zeininger et al.,

No. 5,344,793, to Kamal et al., No. 6,303,503, and to Huang, No. 6,117,723, European Patent Application No. 325328, and the publications of Hong et al., "$CoSi_2$ With Low Diode Leakage and Low Sheet Resistance At 0.065 μm Gate Length, in IEDM 97, pages 107-110, Lee et al., "A High Performance 0.13 μm CMOS Process for ghz Microprocessor Manufacture" in IEEE 6th International Conference of VLSI and CAD (October 1999), pages 136-139, Yan et al., "High Performance 0.1-μm Room Temperature Si MOSFETs", in 1992 Symposium on VLSI Technology Digest of Technical Papers (1992), pages 86 and 87, and Rho et al., Dependence of Deep Submicron CMOSFET Characteristics on Shallow Source/Drain Junction Depth", in International Conference of Microelectronics and VLSI (1995), pages 291-294, under the provisions of 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claims, including, inter alia, forming a conductive film (gate electrode) on an insulating film and isolating element, the conductive film having a width of 0.18 μm or less; forming the first and second semiconductor (source/drain) regions respectively self-aligned with the conductive film (gate electrode) and sidewall spacers formed on side surfaces of the, e.g., gate electrode (e.g., forming LDD structure); and removing the top of the semiconductor substrate and removing the top of the conductive film (gate electrode), to 2.5 nm or less below the surface of the semiconductor substrate and conductive film (gate electrode) respectively, by Ar sputter-etching, with cobalt silicide layers being formed in the surface of semiconductor regions (the second source/drain regions) and the conductive film (gate electrode), wherein the cobalt silicide layers are not formed in contact with junctions formed by the first semiconductor regions (first source/drain

regions) and the semiconductor substrate, so as to prevent the specified current leakage. See claim 103; note also claims 124 and 127.

Noting especially Fig. 8 of Applicants' original disclosure, and the discussion in connection therewith in paragraph [0047] on pages 19 and 20 of Applicants' substitute specification, problems of current leakage are particularly severe in connection with structure found as in the present invention, having, e.g., LDD structure with first semiconductor regions extending beneath the sidewall spacers on sidewalls of gate electrodes. The present invention avoids current leakage problems even in connection with such LDD structure, by processing as in the present claims, as discussed infra.

Furthermore, it is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claims, having features as discussed previously in connection with independent claims 103, 124 and 127, and, moreover, wherein the second semiconductor regions are formed to a depth of 50-150 nm from the top of the semiconductor substrate (see, e.g., claim 146), more specifically approximately 150 nm from the top of the semiconductor substrate (see claim 145); and/or wherein in forming the cobalt silicide layers in the surface of the semiconductor regions, the bottom thereof is formed to be even (see claim 147), and, moreover, wherein in forming the cobalt silicide layers a thickness thereof is uniform (see claim 148).

As is clear from, for example, pages 24 and 25 of Applicants' substitute specification, by forming the cobalt silicide layer as in, e.g., claims 147 and 148, approach of, or penetration of, the junction by the cobalt silicide can be avoided, thereby avoiding current leakage in connection therewith.

In addition, it is respectfully submitted that these references would have neither taught nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claim, having features as discussed previously in connection with independent claims 103, 124 and 127, and, moreover, wherein in removing, inter alia, a top surface of the conductive film (gate electrode), a height of steps of the conductive film (gate electrode) formed over the semiconductor substrate and over the isolation element is reduced (see claims 136-138).

Furthermore, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claims, having features as discussed previously in connection with claims 103, 124 and 127, and, moreover, having additional features as in the remaining dependent claims, including (but not limited to) wherein the isolating region is formed by forming a trench in the semiconductor substrate and depositing an insulating film in the trench (see claims 133-135); and/or wherein the sputter-etching is carried out after the surface of the semiconductor substrate and the conductive film have been cleaned by using hydrofluoric acid as a cleaning agent (see claim 107); and/or wherein the cobalt silicide layers have a thickness as in claims 110 and 130; and/or wherein the top of the conductive film (gate electrode) is sputter-etched simultaneously with the sputter-etching away the top of the semiconductor substrate (see claims 112 and 132).

Furthermore, and as will be discussed further infra, it is respectfully submitted that even assuming, arguendo, that the teachings of the applied prior art would have established a prima facie case of obviousness, the evidence in Applicants' disclosure

shows unexpectedly better results achieved according to the present invention in Ar sputter-etching at most 2.5 nm below the surface of the semiconductor substrate/conductive film (gate electrode), for avoiding current leakage, overcoming any such prima facie case of obviousness and supporting unobviousness of the presently claimed subject matter. This evidence in Applicants' disclosure must be considered in any determination of obviousness. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984).

As for this evidence of unexpectedly better results, attention is respectfully directed to Fig. 9 and the description in connection therewith in paragraphs [0049]-[0051] on pages 20 and 21 of Applicants' Substitute Specification, together with Figs. 10-13 and the description in connection therewith in paragraphs [0054]-[0056] on pages 21-23 of this Substitute Specification. It is respectfully submitted that this evidence shows unexpectedly better results achieved according to the present invention, wherein the sputter-etching etches away only 2.5 nm or less below the surface of the semiconductor substrate and below the surface of the conductive film (gate electrode), overcomes any prima facie case of obviousness, and clearly supports patentability of the presently claimed subject matter.

Thus, Fig. 9 is a graph showing a first set of data to indicate a relationship between the amount of sputter-etching and the yield of products. As shown in line (a) of Fig. 9, a yield of approximately 90% can be ensured by an amount of sputter-etching from among 0, 1, 2, 3 or 4 nm when the critical value of the standby current (Isb) is set to 28 μm or less. However, when the critical value of the standby current (Isb) is set to 5 μA or less as shown in line (b), the yield is improved when the amount of sputter-etching is 1 or 2 nm, as compared with the case where no sputter-etching is carried out (that is, the amount of sputter-etching is 0). Moreover, when

the amount of sputter-etching 3 or 4 nm, the yield becomes lower than in the case where no sputter-etching is carried out; the yield dropped to approximately 0 when the amount of sputter-etching was 4 nm. As is clear from Fig. 9, a semiconductor integrated circuit device for which the amount of sputter-etching is 3 nm or above cannot be adopted for use in products featuring a low consumption of current that have a critical value for standby current (Isb) of 5 μA or less.

As seen in the foregoing paragraph, the amount of sputter-etching according to the present invention provides unexpectedly better results, in being adaptable for use in products featuring a low consumption of current that have a critical value for standby current (Isb) of 5 μA or less.

In addition, attention is respectfully directed to a second set of data shown in Figs. 10-13 and described in paragraphs [0054] - [0056] on pages 21-23 of Applicants' substitute specification. These figures show that when no sputter-etching is carried out (the amount of sputter-etching being 0), there are 197 chips with standby current flows of 3.5-4 μA, as seen in Fig. 10. As depicted in Figs. 11 and 12, when the amount of sputter-etching is 1 nm and 2 nm, respectively, there are 496 chips with standby current flows of 2.5 to 3 μA, and 479 chips with standby current flows of 4 μA or less. As seen in Fig. 13, when the amount of sputter-etching is 3 nm, there are 202 good chips with standby current of 4-4.5 μA. As can be appreciated, the smaller the standby current, the better the performance of a chip; consequently, when the amount of sputter-etching is set to 2.5 nm or less, more chips with lower level of standby current can be obtained, hence more chips with high-levels of performance can be obtained.

It is respectfully submitted, that this evidence shows unexpectedly better results in lower levels of standby current, with higher levels of performance, obtained

according to the present invention, as compared with, for example, sputter-etching at levels greater than that in the present claims or with no sputter-etching.

It is further respectfully submitted that by reducing the standby current of the semiconductor integrated circuit device, consumption of current is reduced. As a result, semiconductor integrated circuit devices formed by the present method are applicable in cellular phones and personal computers which are battery-driven, as they are able to lengthen the times over which these products are used.

Attention is also directed to Fig. 15 of the above-identified application, and the description in connection therewith in paragraph [0064] on pages 25 and 26 of Applicants' substitute specification. As is clear therefrom, when the sputter-etching is undesirably great, for example, greater than 2.5 nm, upon forming the silicide the metal silicide layer approaches the junctions of the source/drain regions, increasing the current leakage. This is avoided according to the present invention; having the sputter-etching to a depth of at most 2.5 nm, such approach to the junction, and resulting increase in the leakage current, can be avoided.

In addition, by etching the surface of the gate electrode by a relatively small thickness (2.5 nm or less), a discontinuity of the layer of metallic silicide can be avoided, so that increase of resistance of the gate electrode layer and a resulting decrease in operation speed, can be avoided. Note paragraphs [0067]-[0069] on pages 26-28 of the Applicants' substitute specification. Moreover, with simultaneous etching of the top of the substrate and the top of the gate electrode, as in various of the present claims (see, e.g., claims 112, 123 and 132), processing is facilitated and simplified.

Again, it is emphasized that the present invention addresses a problem arising especially in connection with the semiconductor integrated circuit devices

having, e.g., LDD structure, with first and second semiconductor regions, wherein current leakage is an especially difficult problem where cobalt silicide layers are provided on the LDD structure. As can especially be appreciated in connection with Fig. 8, the cobalt silicide layer can at least approach, and may even penetrate, junctions having such LDD structure, especially at the more lightly doped implant regions (first semiconductor or source/drain regions) underlying the sidewall spacer. It is respectfully submitted that none of the applied references address this problem of current leakage of structure having LDD implant regions and cobalt silicide layers formed thereon; and it is respectfully submitted that the applied references would have neither disclosed nor would have suggested solutions to such problem of current leakage in connection with such structure, achieved by the present invention.

European Patent Application No. 325,328 discloses a method of manufacturing a semiconductor device, which includes providing a substrate having doped semiconductor regions for forming at least one electrical component, at least one of the doped regions having an exposed surface area, and depositing metal for forming a metal silicide at the exposed area, with the exposed surface area being subjected to sputter-etching prior to depositing the metal to form the metal silicide. This patent document goes on to disclose that the sputter-etching enables oxide to be removed which would, despite conventional chemical wet etching to remove native oxide during previous processing steps, form on the exposed silicon surface area, and that removal of this oxide facilitates formation of the subsequent silicide. Note column 2, lines 4-22. This patent document also discloses that the sputter-etching also forms a layer of amorphous silicon at each exposed silicon surface area; and thus not only does the sputtering remove oxide which can be detrimental to silicide formation, but the disclosed method also provides silicon having the same

or at least a similar physical structure at each exposed surface area. See column 3, lines 2-10. Note also, column 3, lines 23-26, disclosing ions of an inert gas, preferably argon, being used to sputter-etch the exposed surface areas. Note also from column 6, line 48 to column 7, line 8; column 7, lines 12-16, 26-33 and 39-46; and column 8, lines 7-12. As a specific example, this patent document discloses in the paragraph bridging columns 7 and 8, that argon sputter-etching is performed to remove from the substrate a thickness of silicon oxide of the order of 10 nm while providing specified amounts of amorphous silicon, and with argon contamination to a depth within the substrate of less than 20 nm, probably in the region of between 5 and 10 nm. This patent discloses sputter-depositing a layer of refractory metal, of approximately 30-100 nm in thickness. See column 8, lines 12-16. Note also column 9, lines 32-50, emphasizing that the sputter-etching provides an amorphous silicon surface at each exposed surface area so that the metal (e.g., titanium) deposited, is deposited onto the same given type of silicon at each exposed surface, regardless of the type of silicon.

Initially, it is emphasized that according to the method in No. 325,328, the silicon material surface is formed into an amorphous surface. It is respectfully submitted that this disclosure would have neither taught nor would have suggested, and in fact would have taught away from, removing the top of the semiconductor substrate to 2.5 nm or less below the surface of the semiconductor substrate by sputter-etching, as in the present invention, and advantages thereof. It is respectfully suggested that by expressly disclosing formation of an amorphous surface, this would have taught away from removing the substrate surface, by sputter-etching, to the depth as in the present claims.

It is emphasized that No. 325,328 discloses a contamination depth of argon of less than 20 nm, probably in the region of between 5 and 10 nm. Clearly, this disclosure of a contamination depth would have neither taught nor would have suggested the removing as in the present claims, much less such removing to a depth of 2.5 nm or less, and advantages thereof as established by the evidence of record.

Furthermore, it is respectfully submitted that the applied European Patent Application provides a general disclosure with respect to use of sputter-etching in formation of a metal silicide. It is respectfully submitted that this reference does not disclose, nor would have suggested, such a fabrication method as in the present claims, including formation of the first semiconductor regions (first source/drain regions), e.g., having a shallow depth, and problems of current leakage that can arise especially in connection therewith; and would have neither taught nor would have suggested the additional processing according to the present invention of removing, inter alia, the top of the conductive film (gate electrode) to 2.5 nm or less by sputter-etching, and formation of the cobalt silicide, while avoiding the problem of current leakage.

The contention by the Examiner in the second paragraph on pages3 of the Office Action mailed May 20, 2005, that No. 325,328 discloses, inter alia, argon sputter etching of less than 20 nm, thus encompassing less than 2.5 nm, is noted. The Examiner is respectfully challenged to point out the specific description in the applied European patent application for argon sputter-etching which removes the substrate of less than 20 nm. While this applied European patent application discloses argon contamination to a depth within the monocrystalline silicon substrate of less than 20 nm, probably in the region of between 5 and 10 nm, in the paragraph

bridging columns 7 and 8 thereof, it is respectfully submitted that such disclosure does not teach, nor would have suggested, Ar sputter-etching which removes the substrate of less than 20 nm.

Additionally, it is again emphasized that applicants have shown unexpectedly better results achieved through use of the removal, by sputter-etching, of 2.5 nm or less from the top of the semiconductor substrate. Even assuming, arguendo, that the applied European Patent Application disclosed argon sputter-etching of "less than 20 nm", as alleged by the Examiner, such disclosure would not have taught or suggested the unexpectedly better results achieved at removal levels of 2.5 nm or less, particularly in view of the disclosure in the applied European Patent Application of argon contamination "of less than 20 nm, probably in the region of between 5 and 10 nm".

Furthermore, the applied European Patent Application is concerned with sputter-etching the semiconductor substrate. Such disclosure would have neither taught nor would have suggested the removing of the conductive film (gate electrode), to a depth of 2.5 nm or less from the surface thereof, or the unexpectedly better results in preventing current leakage in structure having first and second semiconductor regions respectively self-aligned with the, e.g., gate electrode and sidewall spacers thereon (e.g., LDD structure), and also in avoiding discontinuities at steps of the conductive film.

It is respectfully submitted that the secondary references as applied by the Examiner would not have rectified the deficiencies of the applied European patent application such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Zeininger et al. discloses defect-enhanced $CoSi_2$ formation and improved silicided junctions in deep submicron MOSFETs. According to an aspect described in this patent, a silicon wafer is first pre-cleaned with hydrofluoric acid. After the HF precleaning, the silicon wafer is transferred to a conventional cobalt sputtering tool where it is sputter-cleaned by bombardment with low energy ions. After the sputter cleaning, cobalt metal is deposited on the silicon wafer at room temperature so as to form the $CoSi_2$ layer. Note the paragraph bridging columns 1 and 2 of this patent; see also column 2, lines 39-42 and 58-64.

Kamal et al. discloses processes for the formation of cobalt silicide layers during semiconductor device fabrication, including a sputter etch surface preparation step prior to the cobalt layer deposition step. The sputter etch is described as an argon sputter etch with a DC bias of less than -280 volts, the argon sputter etch process conditions being optimized in order to minimize backsputtering of silicon onto the gate sidewall spacers, while still adequately removing native silicon dioxide from the source region, drain region and silicon gate. The sputter etch is performed to prevent forming a cobalt silicide bridge between the gate electrode and source/drain region. See column 2, lines 48-66. Note also column 3, lines 9-11; and column 5, lines 60-65.

Hong et al. reports on an investigation of effectiveness of four methods for diode leakage reduction and their impact on sub-0.18μm CMOS device performance. This article discloses that key results show (1) pre-Co deposition sputter clean can reduce leakage but only to a certain extent; (2) ion amorphization tightens diode leakage distribution at a cost of increasing source-to-drain series resistance and its extendibility to shallower junctions is questionable; (3) high temperature silicidation significantly improves diode leakage but increases source-to-drain series resistance;

and (4) high temperature Co deposition can improve diode leakage even at low RTP temperatures. Note the paragraph bridging the left-and right-hand columns on page 107. See also the first full paragraph in the right- hand column on page 107.

Lee et al. proposes a highly manufacturable and high performance 0.13 μm CMOS technology to meet the requirements for future gigaherz microprocessor application. The technology includes shallow trench isolation, aggressive doping engineering for threshold adjustment and gate doping, dual gate CMOS transistors, and advanced Co-salicide for low resistance.

Huang discloses a process used to integrate fabrication of logic devices and dynamic random access memory (DRAM) devices on a same semiconductor substrate. This patent discloses formation of a metal silicide layer selectively formed on all exposed regions of silicon or polysilicon, encompassing all gate structures and all heavily doped source/drain regions in the logic device region, while forming the metal silicide layer on the top surface of a blanket of a polysilicon layer in the DRAM region. This patent specifically discloses that the metal silicide is not formed on source/drain regions in the DRAM region, to thereby avoid junction leakage in the DRAM cell. Note, for example, column 2, lines 5-50. See also, for example, column 5, lines 21-27 and 57-61.

Initially, it is emphasized that Huang specifically teaches that the metal silicide is not formed in DRAM structure. It is respectfully submitted that, as applied by the Examiner, the Examiner has ignored express teachings of Huang in connection with preventing metal silicide formation in DRAM regions. It is respectfully submitted that as combined by the Examiner, Huang is destroyed for its intended purpose. Accordingly, it is respectfully submitted that combination of Huang with teachings of other references as applied by the Examiner is improper. See In re Ratti, 123 USPQ

349 (CCPA 1959). Taking the teachings of Huang as a whole, as required under 35 USC 103, it is respectfully submitted that one of ordinary skill in the art would not have combined the teachings of Huang with the teachings of the other references as applied by the Examiner.

In any event, even assuming, arguendo, that the teachings of the references as applied by the Examiner, including Huang, were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed method, including, e.g., the formation of the semiconductor regions respectively self-aligned with the conductive film (gate electrode) and sidewall spacers thereon, and current leakage problems in connection therewith in providing a cobalt silicide film on these semiconductor regions, and avoiding such problem as achieved by the present invention, by the processing recited in the present claims including the removing by Ar sputter etch to a depth of 2.5 nm or less; and/or processing of the conductive film (gate electrode) as in the present claims.

On page 3 of the Office Action mailed May 20, 2005, the Examiner contends that the applied European patent application discloses argon sputter etching of less than 20 nm, and encompasses less than 2.5 nm. As discussed previously, Applicants have found no disclosure in the applied European patent application of removal of the semiconductor substrate, and the Examiner is respectfully requested to point out the specific disclosure in the applied European patent application of such removing. See 35 USC 132.

Moreover, even assuming, arguendo, that the applied European patent application disclosed removal of less than 20 nm, as can be appreciated such maximum depth removed is much greater than the maximum depth according to the present claims. Moreover, it is respectfully submitted that Applicants have shown

unexpectedly better results achieved in removing a maximum depth of 2.5 nm. Particularly in view of the unexpectedly better results achieved according to the present invention, it is respectfully submitted that the teachings of the prior art as applied by the Examiner would have neither disclosed nor would have suggested the presently claimed subject matter.

It is again emphasized that, even as interpreted by the Examiner, the European patent application discloses removal of a much greater depth from the surface of the semiconductor substrate, as compared with that recited in the present claims. It is respectfully submitted that the evidence of record shows unexpectedly better results achieved with respect to depth removed, providing a comparison with the closest prior art, and establishes unobviousness of the presently claimed subject matter, even assuming, arguendo, that the teachings of the applied prior art establishes a prima facie case of obviousness.

The Examiner has also relied on Hong et al. as disclosing removal of 2.5 nm or less of the top of the semiconductor substrate.

It is respectfully submitted that in Hong et al., the purpose of the Ar sputter-clean is to remove silicon surface contaminates (e.g., native oxide). As shown in this article, e.g., in Fig. 2, a longer sputter clean causes plasma damage to the gate oxide film. Moreover, it is respectfully submitted that this document does not disclose implant regions (e.g., the first and second semiconductor regions, or source/drain regions), and current leakage problems arising in connection therewith. It is respectfully submitted that Hong, et al. does not disclose, nor would have suggested, either alone or in combination with the teachings of the other references as applied by the Examiner, problems addressed by to the present invention of

current leakage due to the structure formed, and avoiding such problems as in the present invention.

The contention by the Examiner on page 6 of the Office Action mailed May 20, 2005, that the associated reduced leakage current would be obtained with ultra shallow sputter etching as readily apparent in Hong et al., is respectfully traversed, particularly with respect to the structure formed by the presently claimed processing, including the semiconductor regions formed. Particularly since Hong et al. does not disclose nor would have suggested formation of first and second semiconductor (source/drain) regions as in the present claims, a basis by the Examiner for the conclusion that reduced current leakage would be obtained in the view of the teachings of Hong et al., is not seen.

The contention by the Examiner on page 4 of the Office Action mailed May 20, 2005, that Kamal et al. discloses removal of 20 angstroms, as the extent of the etching, the Examiner referring to line 65 of column 5 of this patent, is noted. It is respectfully submitted, however, that at column 5, line 65, Kamal et al. discloses removal of native silicon dioxide of between 20 and 60 angstroms. It is respectfully submitted that this reference would not have disclosed, nor would have suggested, a maximum removal of 2.5 nm, below the surface of the semiconductor substrate, and advantages achieved thereby as discussed in the foregoing; and clearly would have neither disclosed nor would have suggested the unexpectedly better results achieved according to the present invention, with maximum removal below the surface of the semiconductor substrate as in the present claims.

Furthermore, the Examiner has not even alleged a removal of an amount from the top surface of the conductor film/gate electrode as in all of the claims presently being considered on the merits. It is respectfully submitted that the applied

references would have neither taught nor would have suggested such removal of the conductive film (gate electrode) as in the present claims, and advantages thereof as discussed in the foregoing.

The article by Rho et al. discloses a new technique named MOSES (Mask Oxide Sidewall Etch Scheme) for fine gate patterning of 0.1 μm dimensions. See the first full paragraph in the right-hand column on page 291,and the paragraph bridging pages 291 and 292). It is disclosed that optimized channel implants are performed with the concept of vertical doping engineering, after conventional well and LOCOS isolation processing.

Yan et al. discloses the design and implementation of 0.15 μm channel N-MOSFETs with very high current drive and good short channel behavior at room temperature. The MOSFETs were fabricated using e-beam lithography for gate definition and self-aligned $TiSi_2$ silicides to reduce parasitic resistances. See the paragraph bridging the left- and right-hand columns on page 86 of this article.

Even assuming, arguendo, that the teachings of Rho et al. or Yan et al. were properly combinable with the teachings of the other documents as applied by the Examiner, it is respectfully submitted that the combined teachings of these documents would have neither disclosed nor would have suggested the presently claimed process, including formation of the semiconductor (source/drain) regions with formation of the cobalt silicide, and current leakage problems in connection therewith, as discussed previously; and avoiding such problems utilizing the removal by Ar sputter-etching of the top surface of the substrate and conductive film (gate electrode) of the maximum depth, and formation of the cobalt silicide layer avoiding contact with the junctions formed by the first semiconductor (source/drain) regions and the semiconductor substrate, as in the present claims, and, in particular, the

unexpectedly better results achieved by the maximum removal of the substrate as in the present claims and/or the maximum removal of the conductive film (gate electrode) and advantages thereof; and/or the other features of the present invention, and advantages thereof, as discussed previously.

Again, Applicants refer to the unexpectedly better results achieved according to the present invention, as seen from the evidence of record. Particularly in view thereof, it is respectfully submitted, that the teachings of the applied documents would have neither disclosed nor would have suggested the presently claimed invention, under the requirements of 35 USC 102 and 35 USC 103.

The rejection of claims 139-144 under the second paragraph of 35 USC 112, as set forth in the first and second paragraphs on page 2 of the Office Action mailed May 20, 2005, is moot, in view of canceling of these claims.

In view of the foregoing comments and amendments, and in view of the concurrently filed RCE Transmittal, entry of the present amendments, and reconsideration and allowance of all claims being considered on the merits in the application, are respectfully requested.

Please charge any shortage of fees due in connection with the filing of this paper to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account. No. 01-2135 (case 501.40724X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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